ECE 304

Lesson #*n*

Why do the slides look like this?

(New) Faculty Forum - February 5, 2013

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Midterm Exam #1

- Friday, February 8, in class
- “Practical” circuit problems
- “Theory” concept/explanation problems
- Problem sets, Review packages, textbook readings

Recent handouts

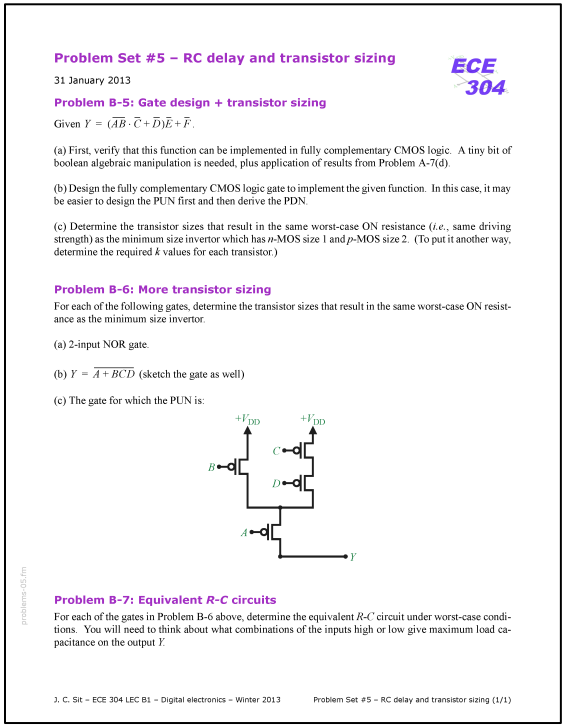
- Problem Set #5
- Midterm Exam #1 – Review
- Midterm Exam #1 – Information
- Introduction – Part B
- Review – Part B (*website*)

New handouts

- Midterm #1 – Review problems
- Problem Set #5
- Problem Set #5 solutions (*website*)

Problem Set #5

- Handed out today
- Also available on course website
- Problems on *R*-*C* delay and transistor sizing



Problem Set #5 – RC delay and transistor sizing

ECE 304

31 January 2013

Problem B-5: Gate design + transistor sizing

Given $Y = (\overline{AB} \cdot \overline{C} + \overline{D})\overline{E} + \overline{F}$.

(a) First, verify that this function can be implemented in fully complementary CMOS logic. A tiny bit of boolean algebraic manipulation is needed, plus application of results from Problem A-7(d).

(b) Design the fully complementary CMOS logic gate to implement the given function. In this case, it may be easier to design the PUN first and then derive the PDN.

(c) Determine the transistor sizes that result in the same worst-case ON resistance (*i.e.*, same driving strength) as the minimum size invertor which has *n*-MOS size 1 and *p*-MOS size 2. (To put it another way, determine the required *k* values for each transistor.)

Problem B-6: More transistor sizing

For each of the following gates, determine the transistor sizes that result in the same worst-case ON resistance as the minimum size invertor.

(a) 2-input NOR gate.

(b) $Y = \overline{A + BCD}$ (sketch the gate as well)

(c) The gate for which the PUN is:

problems-05.fm

Problem B-7: Equivalent *R-C* circuits

For each of the gates in Problem B-6 above, determine the equivalent *R*-*C* circuit under worst-case conditions. You will need to think about what combinations of the inputs high or low give maximum load capacitance on the output *Y*.

J. C. Sit – ECE 304 LEC B1 – Digital electronics – Winter 2013 Problem Set #5 – RC delay and transistor sizing (1/1)

Course website

- URL: *`http://ece304.jsit.ca`*
- Username: **`student`**
- Password: **`Digital101`** (note: case sensitive)
- Please visit often

Summary of last class

- Using the simplified *R*-*C* model
  - *R* scales inversely with *W*; *C* scales directly with *W*
- Replace FETs with *R*-*C* models
- Simplify the *R*-*C* circuit

A.5 Pass-transistor logic and trans. gates

- the “bad” non-invertor (buffer)
  - strong vs. degraded 1s and 0s
- the transmission gate
- pass-transistor logic

A.5.3 Pass-transistor logic

- Consider a 2:1 multiplexor

A.L.E.

- Write down function $Y = f(S, P, Q)$.
- List all possible functions of one variable $Y = f(S)$.

Prob A-15: AND gate

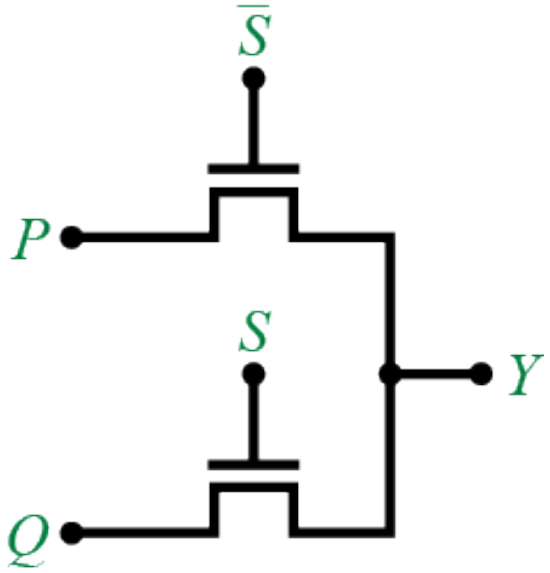
Implement an AND gate $Y = AB$

a) Implement using fully complementary static CMOS logic. How many transistors are required?

AND = NOT NAND

Prob A-15: AND gate

b) Use 2:1 multiplexors...



Prob A-15: AND gate

c) Use 2:1 multiplexors...

B.1.4 Transistor sizing

- We want to design logic gates so that their delay is the same or better than the unit width invertor.
- This means the pull-up and pull-down resistance must be $\leq R$ in all cases.

Prob B-4: Complex gate transistor sizing

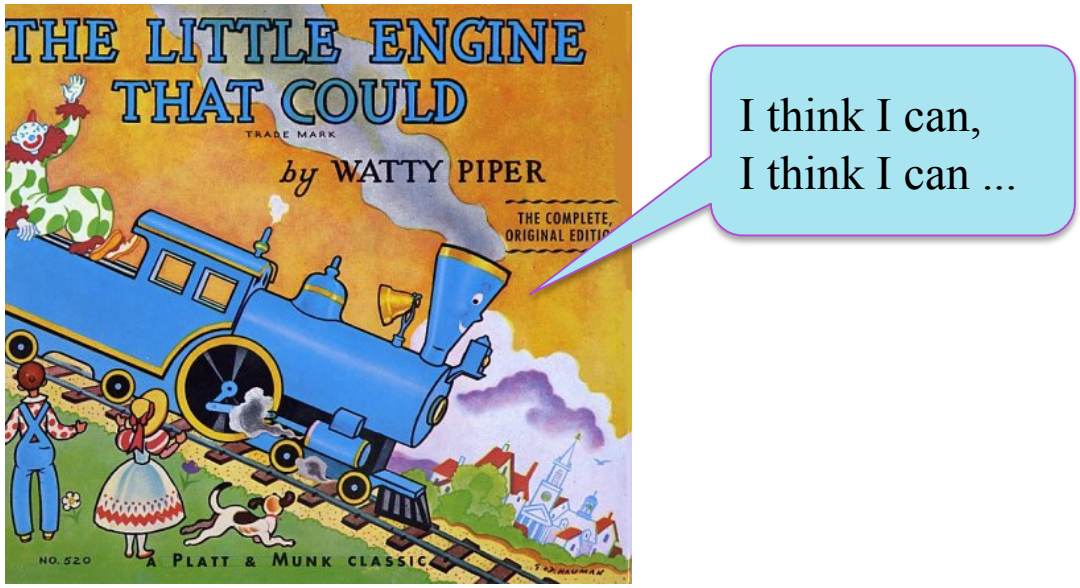
- Size the transistors appropriately...

B.1.5 Elmore delay

- Approximate the delay of a complex R-C network "tree".
- Easiest to understand by looking at examples.

B.1.6 Logical effort

- Text:
  - 3rd ed. §4.2~4.3
  - 4th ed. §4.3~4.5



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